TFT LCD Approval Specification

MODEL NO.: V470H1 – LH2

Customer: Nexgen

Approved by:

Note:

Approved By	TV Head Division
	LY Chen

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

-

Prepared By	LCD TV Marketing and Product Management Div	
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CONTENTS

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver.2.0	Dec,01,08'	All	All	Approval specification was first issued
Ver.2.1	Jul,06,09'	P.26	7.2	OPTICAL SPECIFICATIONS
		P1	cover	Modify the owner of QA Dept. and LCD TV Marketing and Product Management Div.
		P11	3.2.3	Modify the range of Internal PWM Control Voltage
		P4	1.4	Modify the Pixel Pitch

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V470H1-LH2 is a 47" TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 1.0G colors (10-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (450 nits)
- High contrast ratio (2000:1)
- Fast response time (Gray to Gray average 4 ms)
- High color saturation (NTSC 88%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1039.68(H) x 584.82(V) (47" diagonal)	mm	(1)
Bezel Opening Area	1049(H) x 593(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.5415 (V) x 0.1805(H)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.0G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 25%) Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1096	-	mm	(1), (2)
	Vertical (V)	-	640	-	mm	
	Depth (D)	-	52.7	-	mm	
Weight		-	15500	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	50	ºC	(1)(2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3)(5)
		Z axis	-	35	G	(3)(5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4)(5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

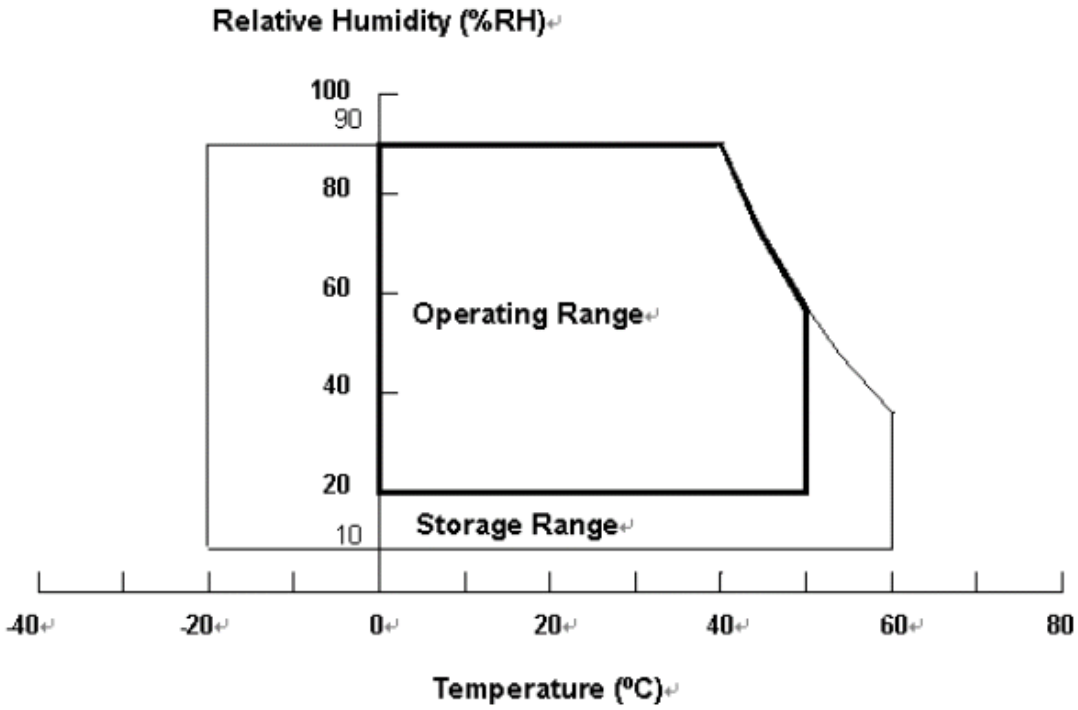
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.2	V	
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

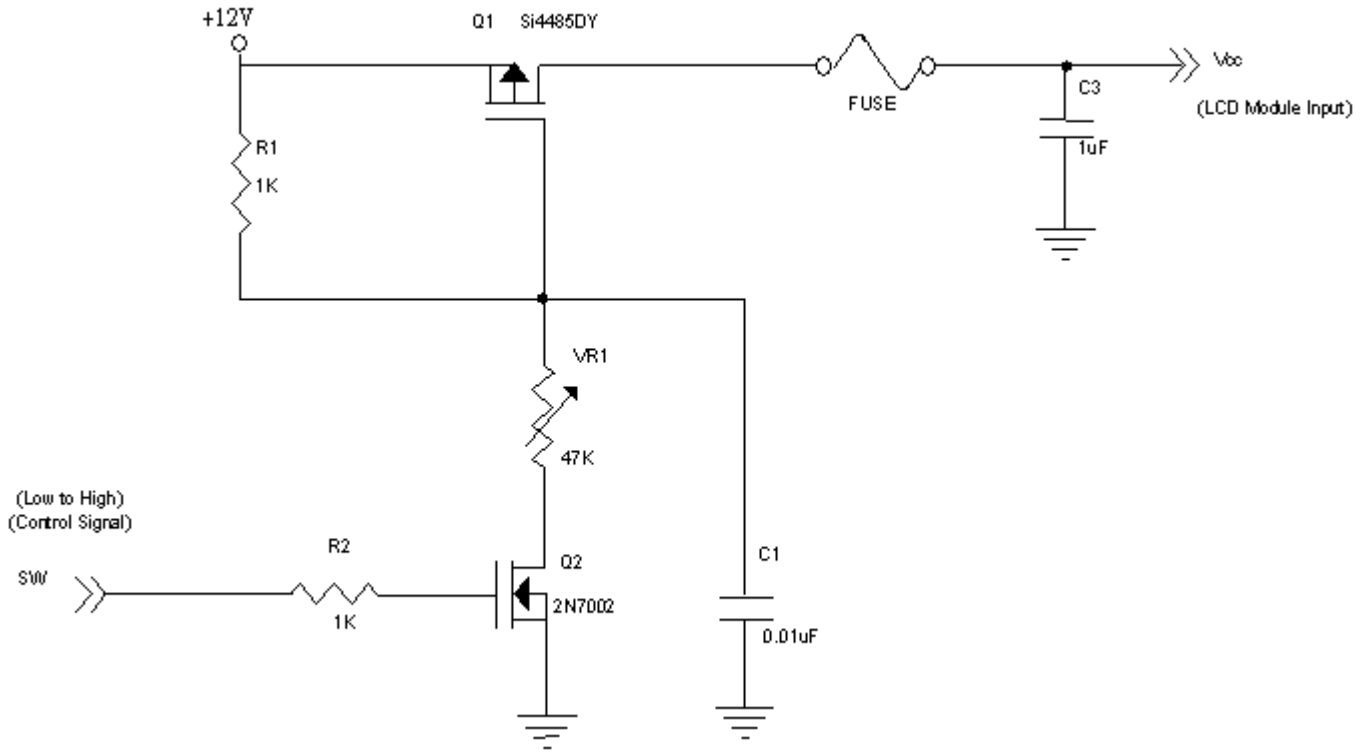
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 ºC)

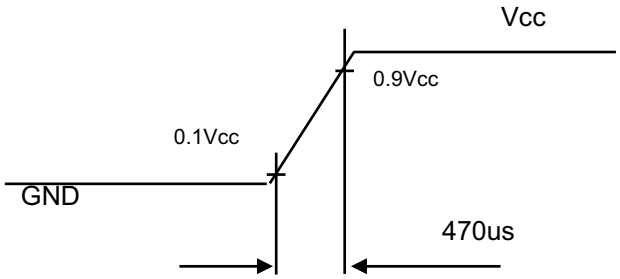
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	-	7.0	A	(2)
Power Supply Current	White	I_{CC}	-	2.5	3.0	A	(3)
	Black		-	1.5	-	A	
	Vertical Stripe		-	2.0	-	A	
LVDS Interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

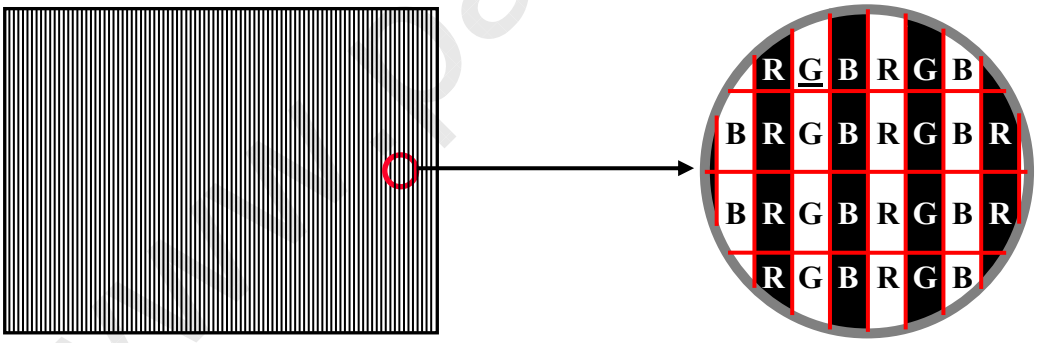
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1400	-	V_{RMS}	-
Lamp Current	I_L	7.5	8.0	8.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2050	V_{RMS}	(2), Ta = 0 ºC
		-	-	1890	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	40	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	197	206	W	(3)(4), I_L = 8.0mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	8.2	8.6	A	
Input Ripple Noise	-	-	-	912	mV_{P-P}	V_{BL}=22.8V
Oscillating Frequency	F_W	37	40	43	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

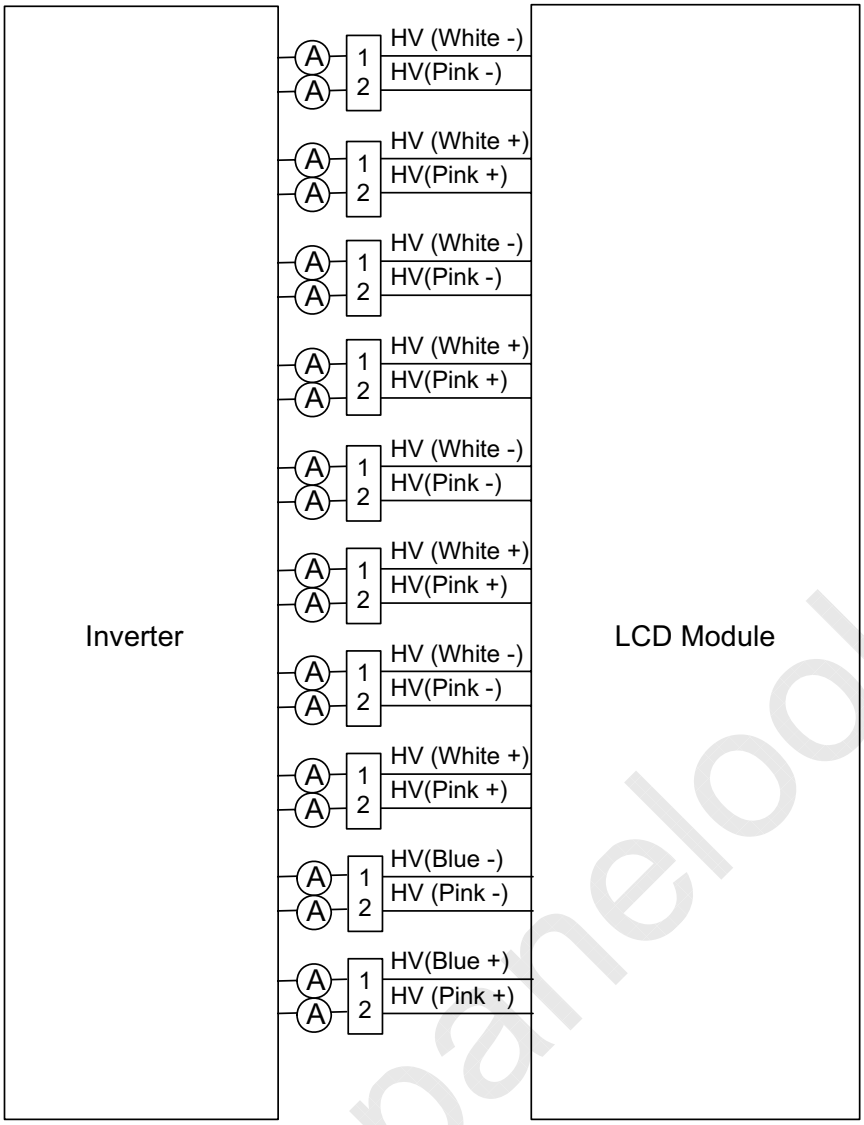
Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 7.5~ 8.5mArms.

Note (5) The measurement condition of Max. value is based on 47" backlight unit under input voltage 24V, average lamp current 8.3 mA and lighting 30 minutes later.



3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Status Signal	HI	States	—	3.0	3.3	3.6	V	Normal
	LO		—	0		0.8	V	Abnormal
Internal PWM Control Voltage	MAX	V_{IPWM}	—	3.15	—	5	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	—	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
PWM Delay Time		T_{PWM}	—	100		—	ms	
BLON Delay Time		T_{on1}	—	300	—	—	ms	
BLON Off Time		T_{OFF}	—	300	—	—	ms	

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

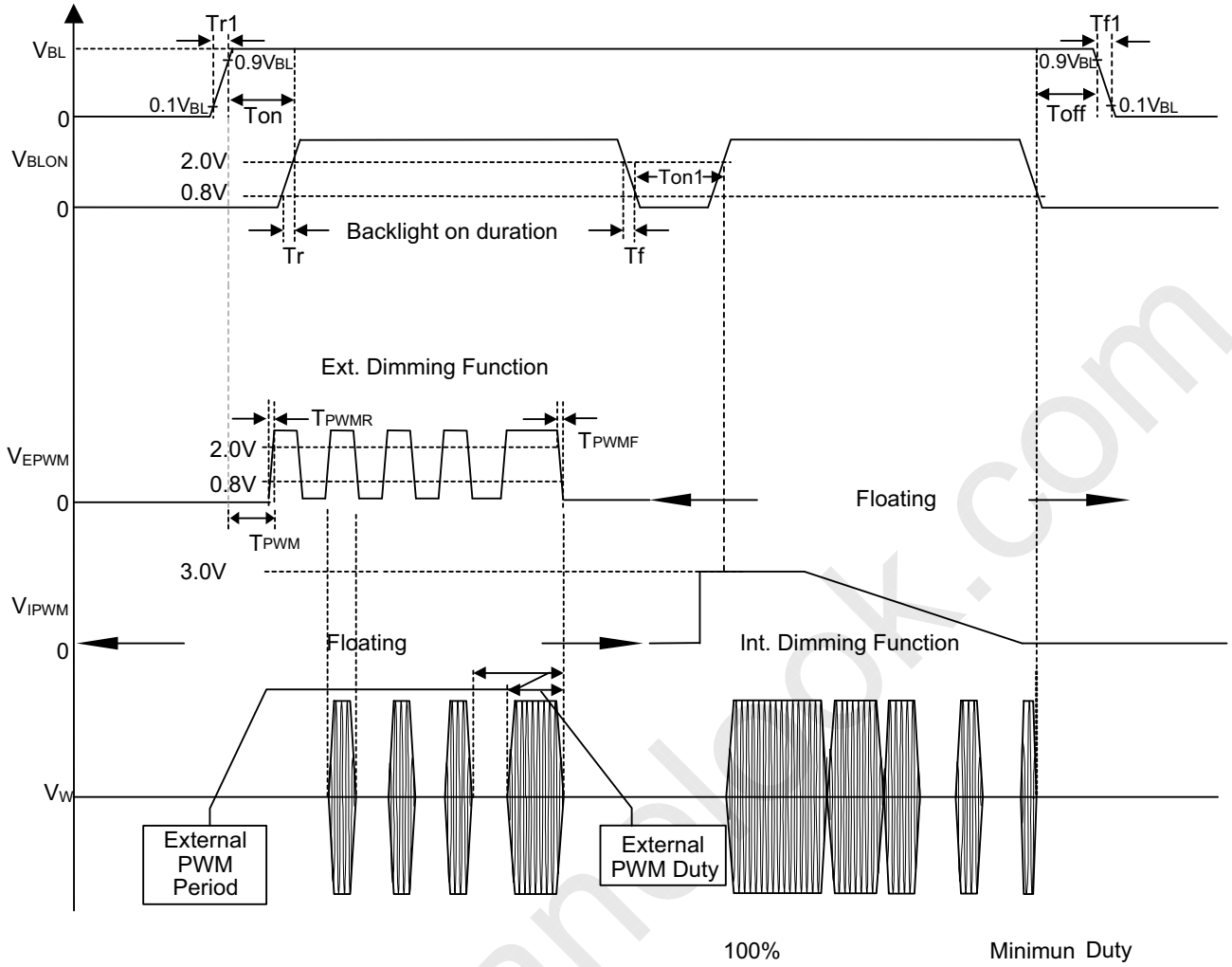
Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

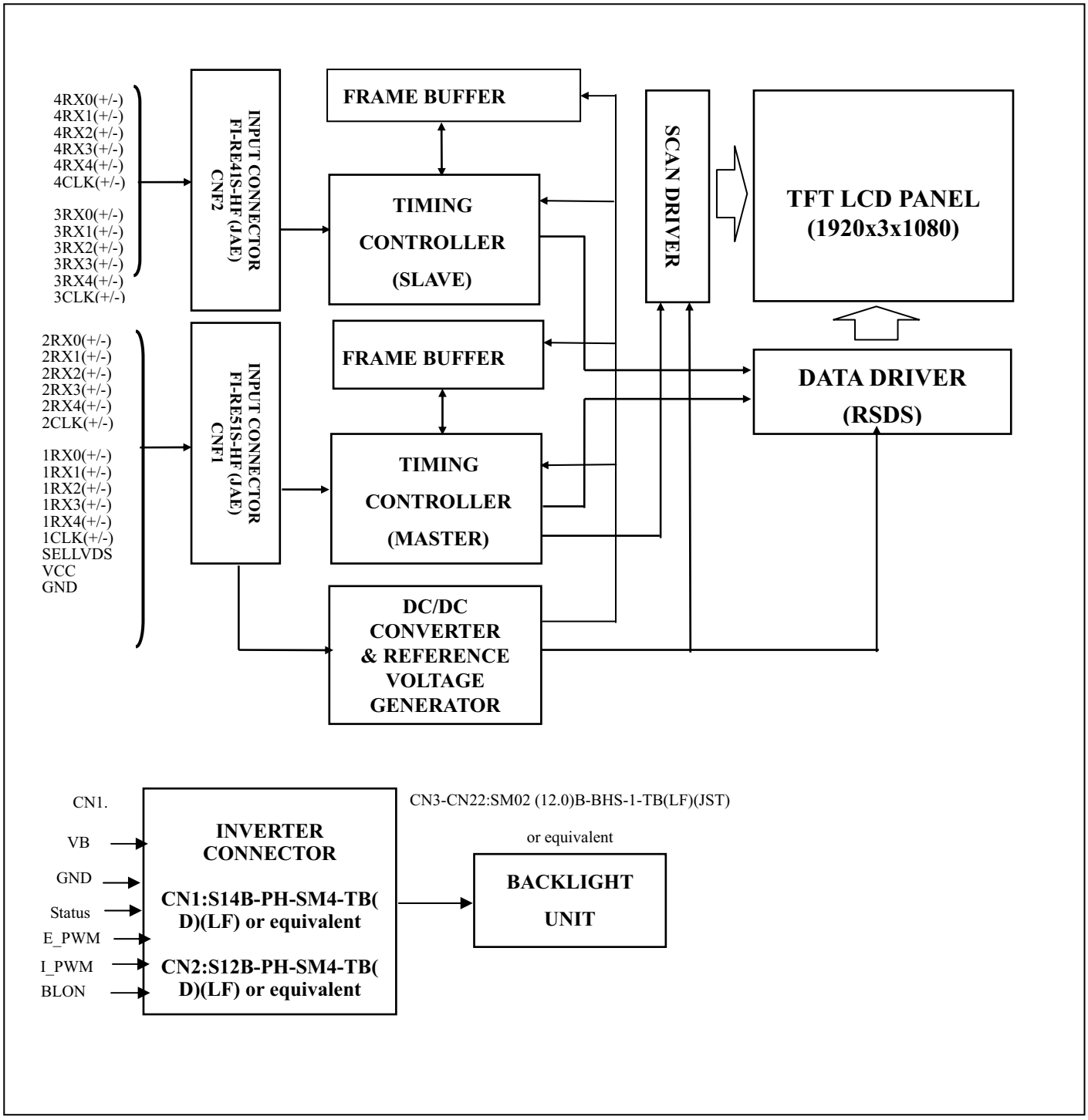
Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) In order to avoid the abnormal phenomenon at dimming condition, skipped range of VIPWM 2.85~3.15V is suggested.



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

CNF1 Connector Pin Assignment(FI-RE51S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS data format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	
11	GND	Ground	
12	RxAo-	First pixel, Negative LVDS differential data input. Channel 0	(3)
13	RxAo+	First pixel, Positive LVDS differential data input. Channel 0	
14	RxBo-	First pixel, Negative LVDS differential data input. Channel 1	
15	RxBo+	First pixel, Positive LVDS differential data input. Channel 1	
16	RxCo-	First pixel, Negative LVDS differential data input. Channel 2	
17	RxCo+	First pixel, Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	RxClko-	First pixel, Negative LVDS differential clock input.	
20	RxClko+	First pixel, Positive LVDS differential clock input.	
21	GND	Ground	
22	RxDo-	First pixel, Negative LVDS differential data input. Channel 3	(3)
23	RxDo+	First pixel, Positive LVDS differential data input. Channel 3	
24	RxEo-	First pixel, Negative LVDS differential data input. Channel 4	
25	RxEo+	First pixel, Positive LVDS differential data input. Channel 4	
26	NC	No Connection	(1)
27	NC	No Connection	(1)
28	RxAe-	Second pixel, Negative LVDS differential data input. Channel 0	(3)
29	RxAe+	Second pixel, Positive LVDS differential data input. Channel 0	
30	RxBe-	Second pixel, Negative LVDS differential data input. Channel 1	
31	RxBe+	Second pixel, Positive LVDS differential data input. Channel 1	
32	RxCe-	Second pixel, Negative LVDS differential data input. Channel 2	
33	RxCe+	Second pixel, Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	RxClke-	Second pixel, Negative LVDS differential clock input.	
36	RxClke+	Second pixel, Positive LVDS differential clock input.	
37	GND	Ground	
38	RxDe-	Second pixel, Negative LVDS differential data input. Channel 3	(3)
39	RxDe+	Second pixel, Positive LVDS differential data input. Channel 3	
40	RxEe-	Second pixel, Negative LVDS differential data input. Channel 4	
41	RxEe+	Second pixel, Positive LVDS differential data input. Channel 4	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	Vin	Power input (+12V)	
49	Vin	Power input (+12V)	

50	Vin	Power input (+12V)	
51	Vin	Power input (+12V)	

CNF2 Connector Pin Assignment (FI-RE41S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	NC	No Connection	(1)
8	N.C.	No Connection	(1)
9	GND	Ground	
10	RxAo-	Third pixel, Negative LVDS differential data input. Channel 0	(3)
11	RxAo+	Third pixel, Positive LVDS differential data input. Channel 0	
12	RxBo-	Third pixel, Negative LVDS differential data input. Channel 1	
13	RxBo+	Third pixel, Positive LVDS differential data input. Channel 1	
14	RxCo-	Third pixel, Negative LVDS differential data input. Channel 2	
15	RxCo+	Third pixel, Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	RxClko-	Third pixel, Negative LVDS differential clock input.	
18	RxClko+	Third pixel, Positive LVDS differential clock input.	
19	GND	Ground	
20	RxDo-	Third pixel, Negative LVDS differential data input. Channel 3	
21	RxDo+	Third pixel, Positive LVDS differential data input. Channel 3	
22	RxEo-	Third pixel, Negative LVDS differential data input. Channel 4	
23	RxEo+	Third pixel, Positive LVDS differential data input. Channel 4	
24	NC	No Connection	(1)
25	NC	No Connection	(1)
26	RxAe-	Fourth pixel, Negative LVDS differential data input. Channel 0	(3)
27	RxAe+	Fourth pixel, Positive LVDS differential data input. Channel 0	
28	RxBe-	Fourth pixel, Negative LVDS differential data input. Channel 1	
29	RxBe+	Fourth pixel, Positive LVDS differential data input. Channel 1	
30	RxCe-	Fourth pixel, Negative LVDS differential data input. Channel 2	
31	RxCe+	Fourth pixel, Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	RxClke-	Fourth pixel, Negative LVDS differential clock input.	
34	RxClke+	Fourth pixel, Positive LVDS differential clock input.	
35	GND	Ground	
36	RxDe-	Fourth pixel, Negative LVDS differential data input. Channel 3	(3)
37	RxDe+	Fourth pixel, Positive LVDS differential data input. Channel 3	
38	RxEe-	Fourth pixel, Negative LVDS differential data input. Channel 4	
39	RxEe+	Fourth pixel, Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Please be reserved to open.

Note (2) Low or Open : VESA LVDS Format (default), High : JEIDA Format.

Note (3) LVDS 4-Port Data Mapping

Port	CH of LVDS	Data Stream
1st Port	First pixel	1, 5, 9, ..., 1913, 1917
2nd Port	Second pixel	2, 6, 10, ..., 1914, 1918
3rd Port	Third pixel	3, 7, 11, ..., 1915, 1919
4th Port	Fourth pixel	4, 8, 12, ..., 1916, 1920

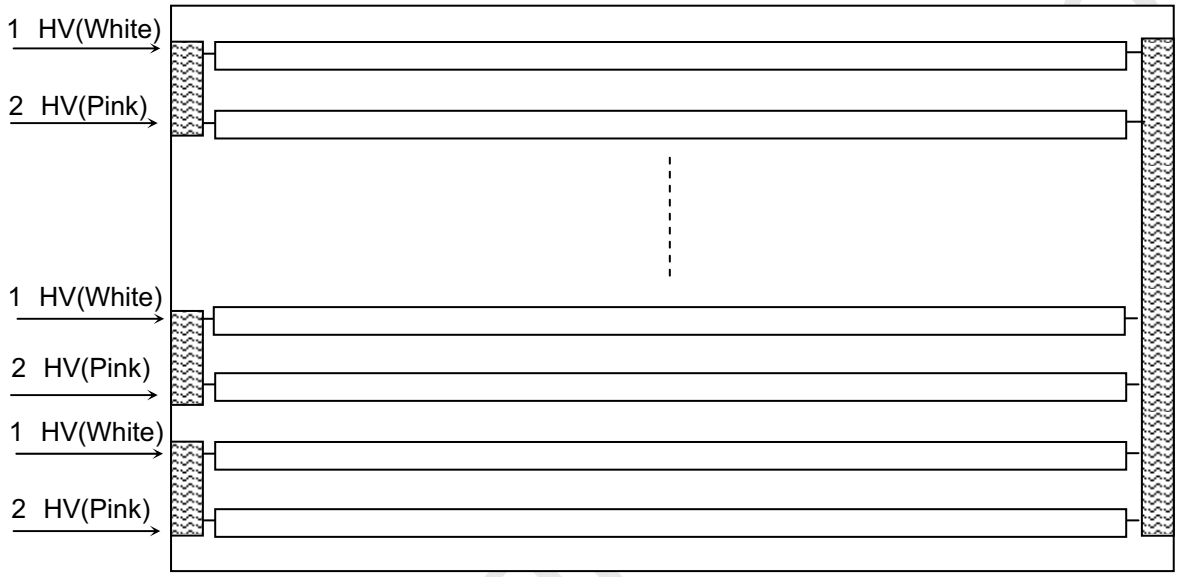
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN22: BHR-04VS-1 (JST). or equivalent

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST. The mating header on inverter part number is SM02 (12.0)B-BHS-1-TB(LF). or equivalent



5.3 INVERTER UNIT

CN1 (Header): S14B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	Status	Normal (3.3V) Abnormal (GND)
12	E_PWM	External PWM control signal
13	I_PWM	Internal PWM Control Signal
14	BLON	Backlight on/off control

Notice:
1. PIN 12:External PWM Control (Use Pin 12): Pin 13 must open.
2. PIN 13:Intermal PWM Control (Use Pin 13): Pin 12 must open.
3. Pin 12(E_PWM) and Pin 13(I_PWM) can't open in same period.

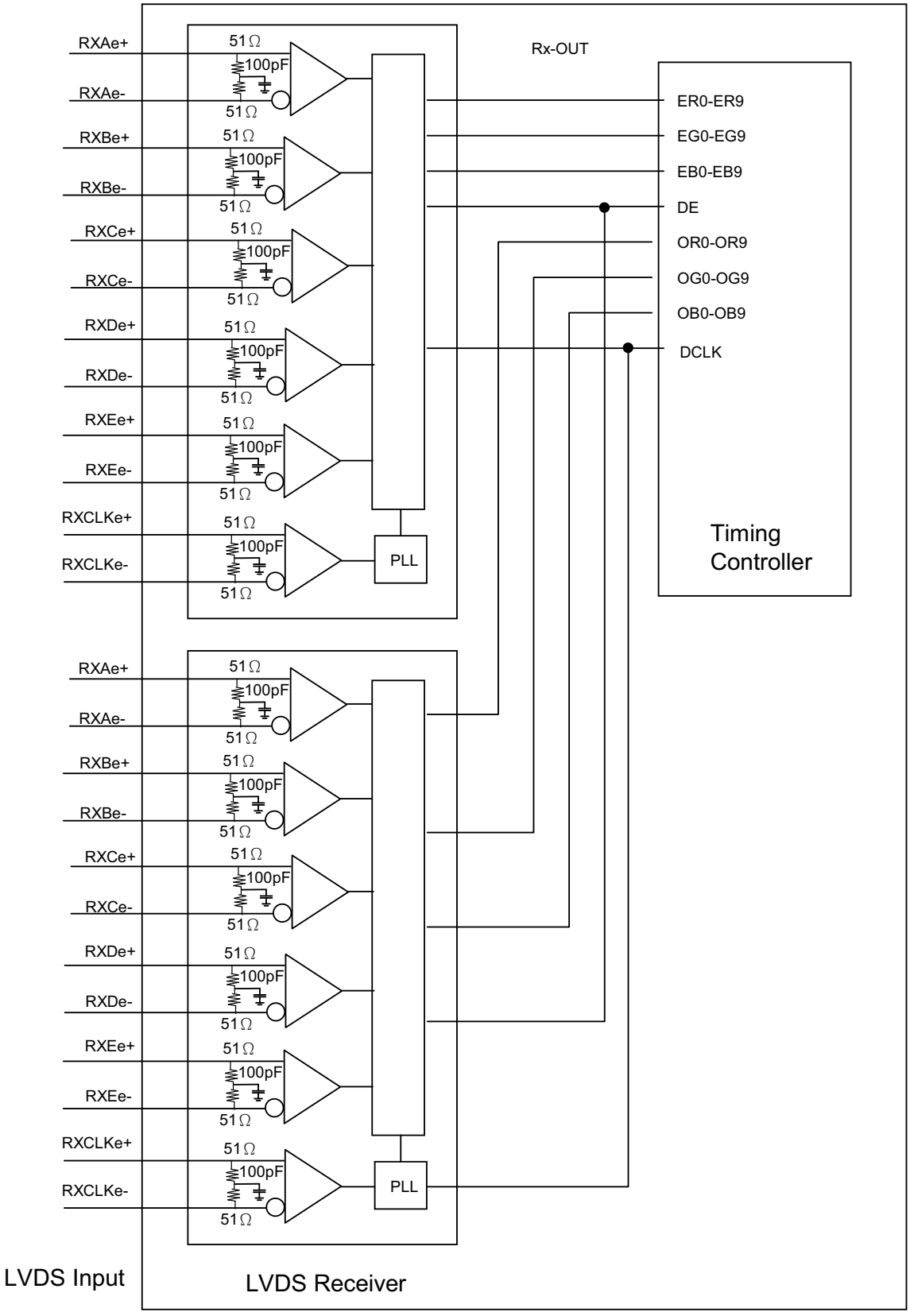
CN2 (Header): S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3-CN22 (Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

5.4 BLOCK DIAGRAM OF INTERFACE

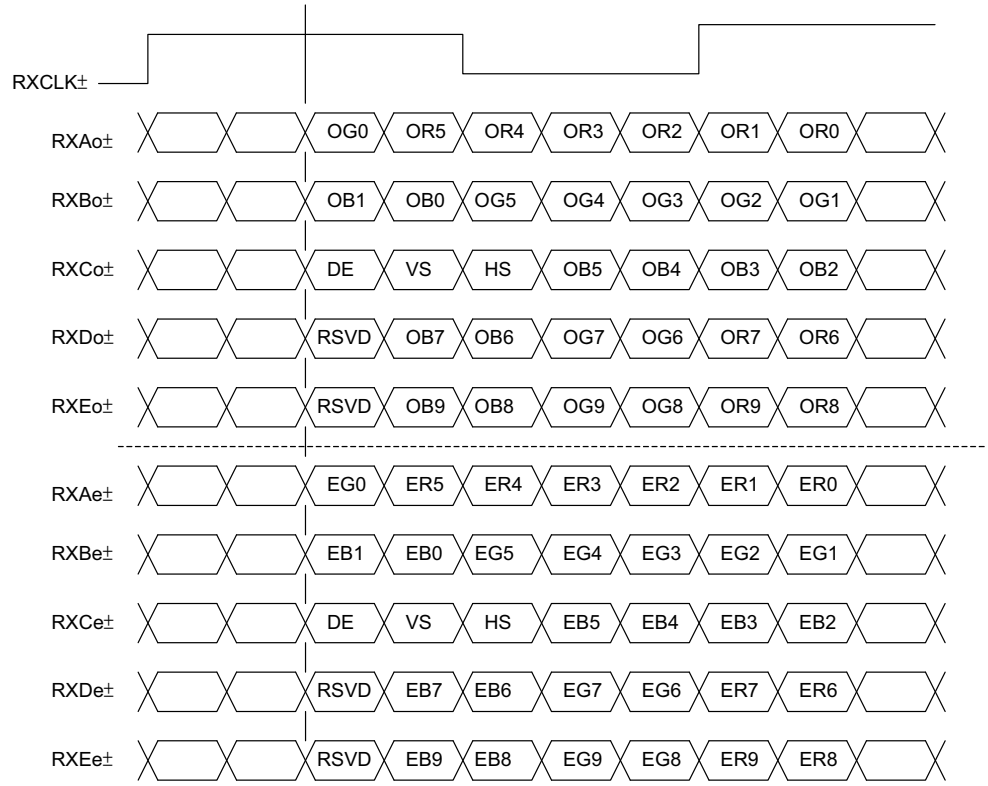


ER0~ER9 : Even pixel R data
EG0~EG9 : Even pixel G data
EB0~EB9 : Even pixel B data
OR0~OR9 : Odd pixel R data
OG0~OG9: Odd pixel G data
OB0~OB9 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

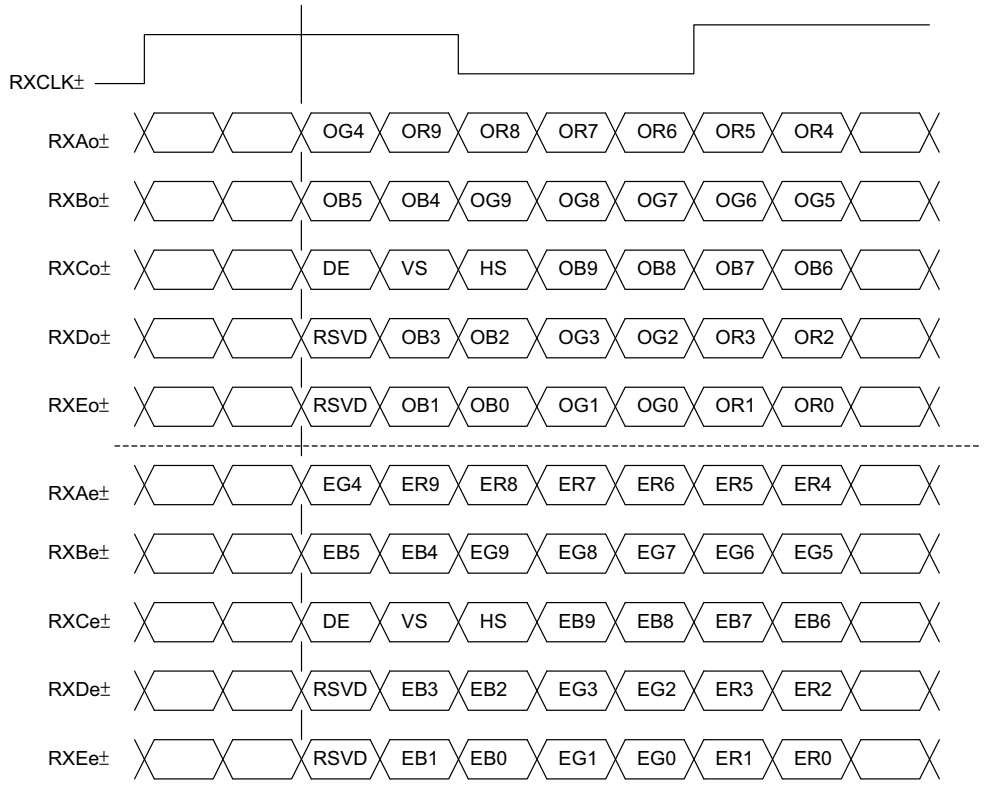
Notes: (1) The system must have the transmitter to drive the module.
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

SELLVDS = L or Open



LVDS_SEL = H



B0~B9: Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

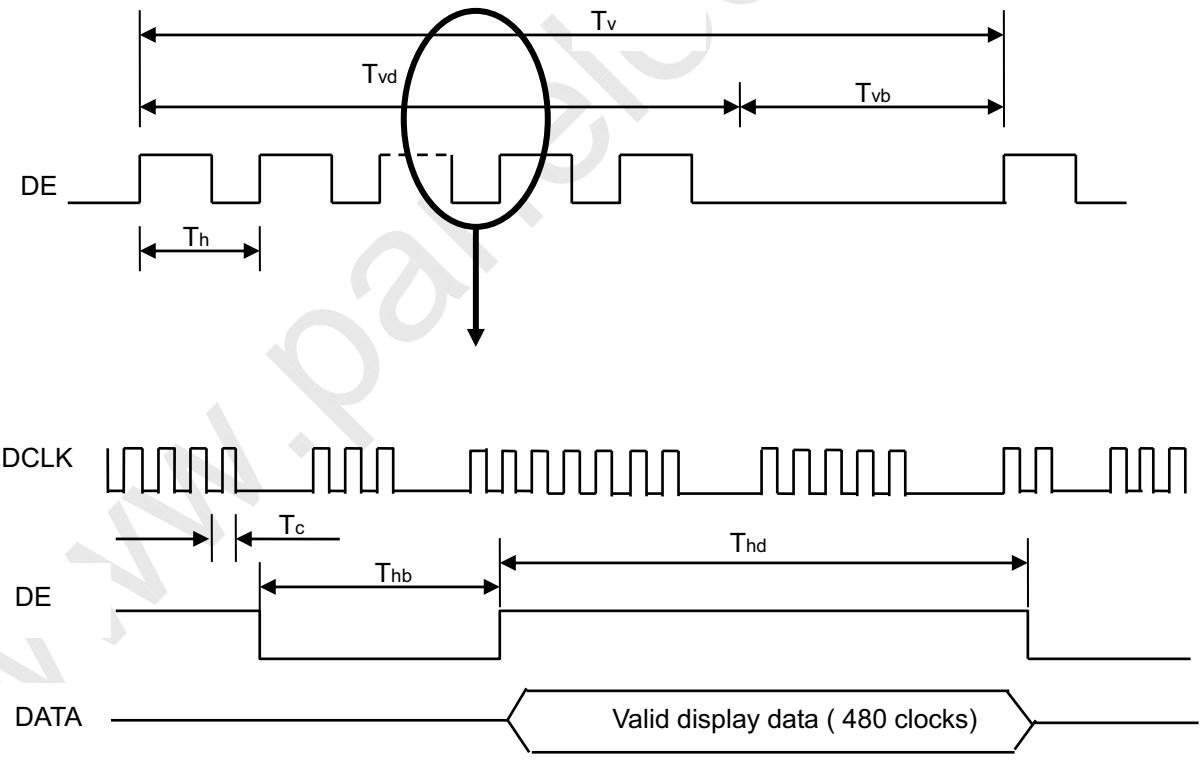
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

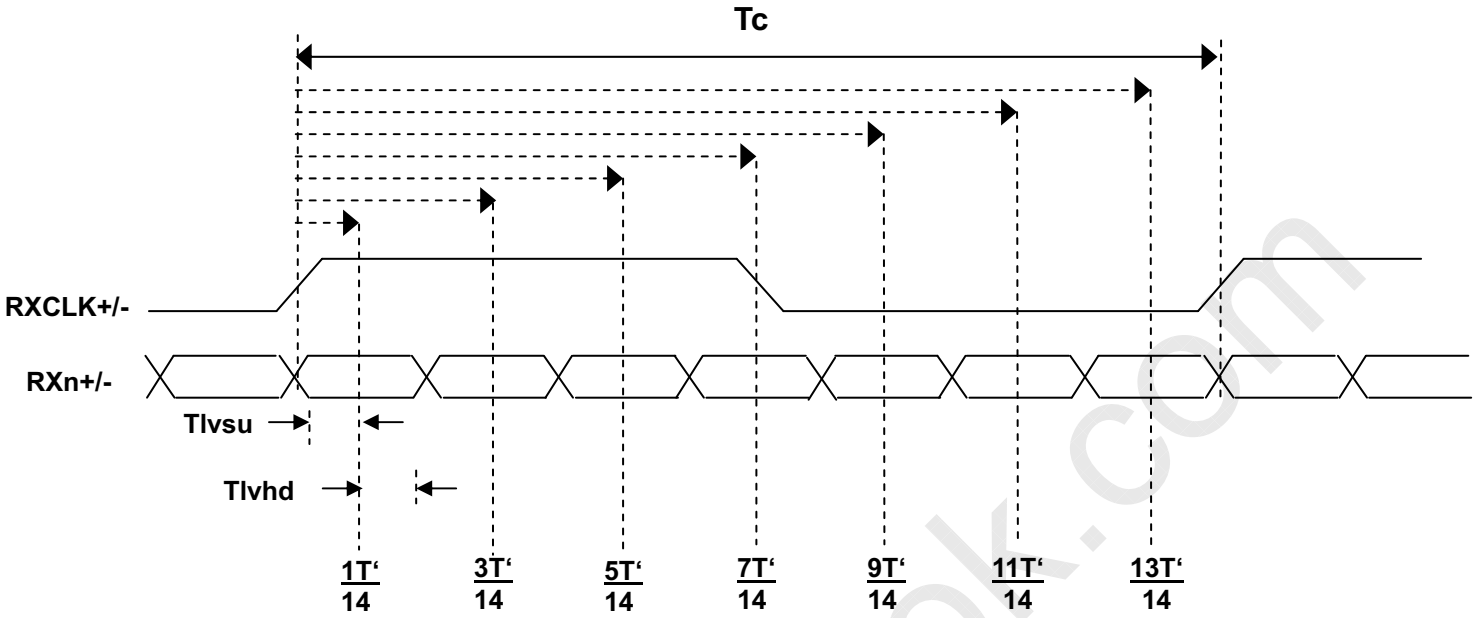
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80	MHz	=297/4
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr	-	120	-	Hz	(1)
	Total	Tv	1115	1125	1139	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	59	Th	-
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	45	70	95	Tc	-

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally..

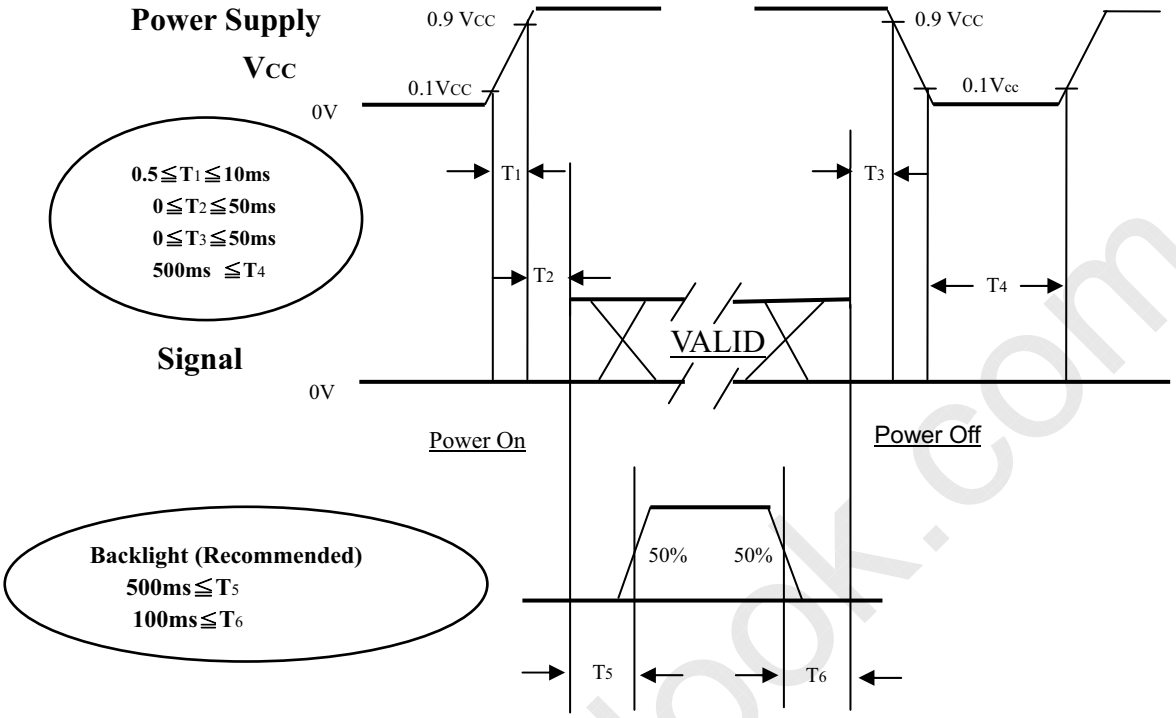
INPUT SIGNAL TIMING DIAGRAM



LVDS INPUT INTERFACE TIMING DIAGRAM

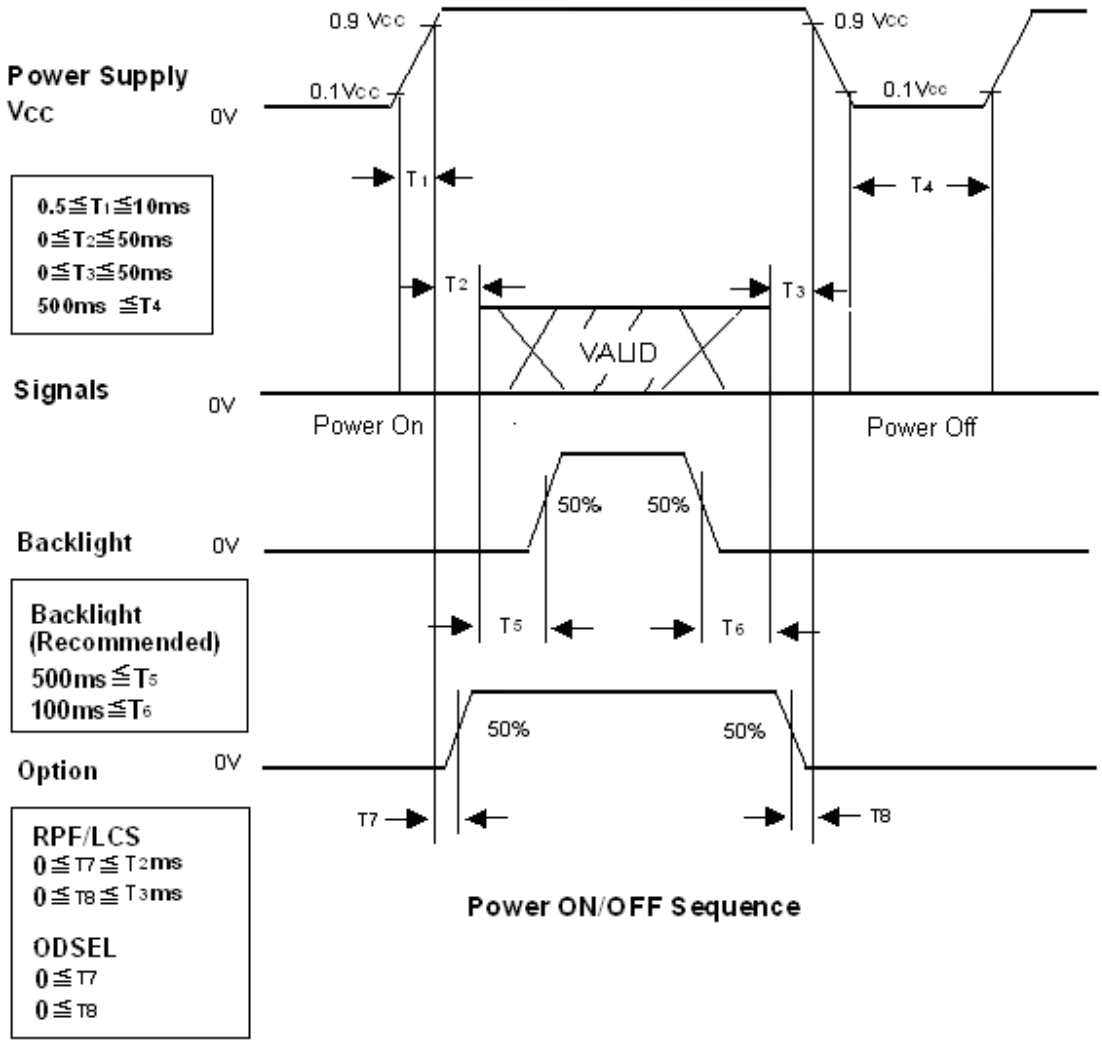


6.2 POWER ON/OFF SEQUENCE



Power ON/OFF Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen. There is no reliability issue when the T5, T6 timing missing the range.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	8.5±0.5	mA
Oscillating Frequency (Inverter)	F_W	40±3	KHz
Vertical Frame Rate	Fr	120	Hz

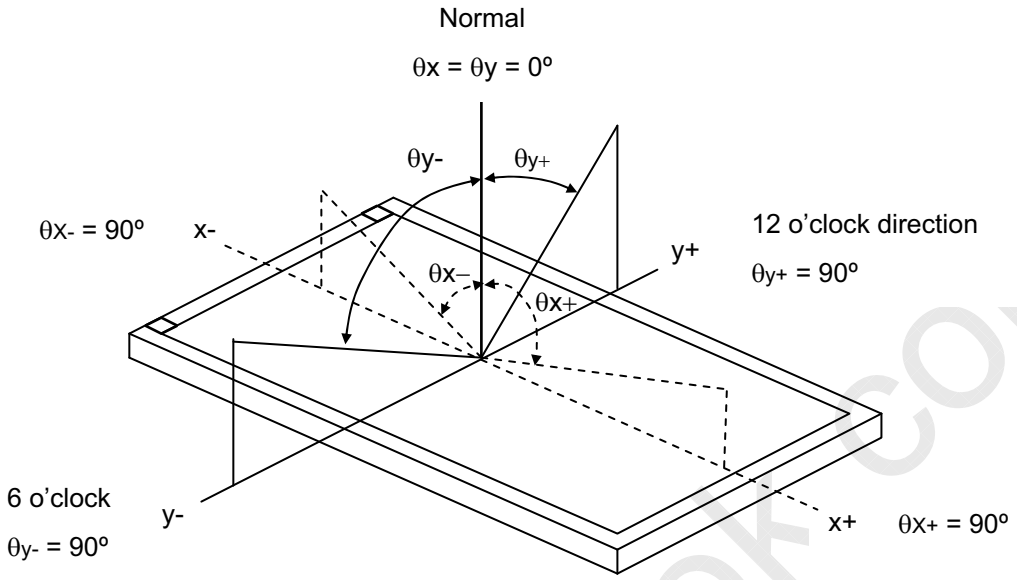
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction	1200	2000	-	-	Note (2)
Response Time		Gray to gray		-	4	-	ms	Note (3)
Center Luminance of White		L_C		380	450	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ.-0.03	0.649	Typ.+0.03	-	Note (6)
		Ry			0.326		-	
	Green	Gx			0.201		-	
		Gy			0.665		-	
	Blue	Bx			0.153		-	
		By			0.066		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut			--	88	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

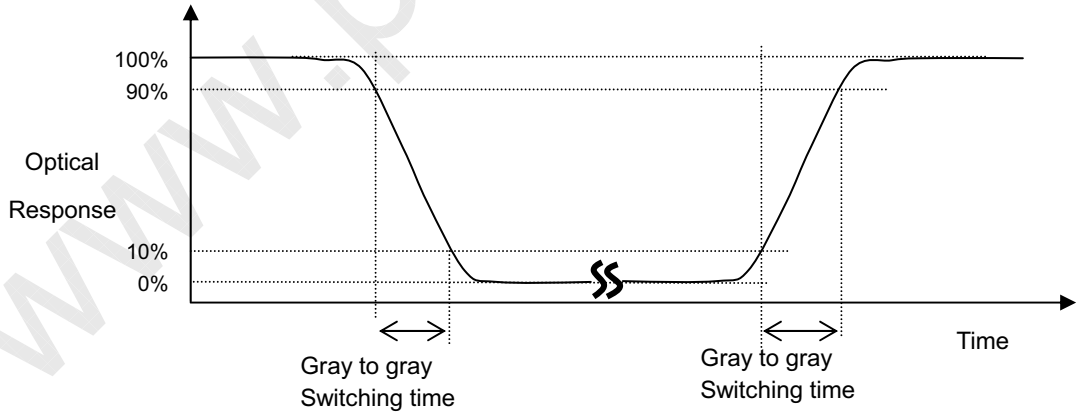
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63,127,191,255 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

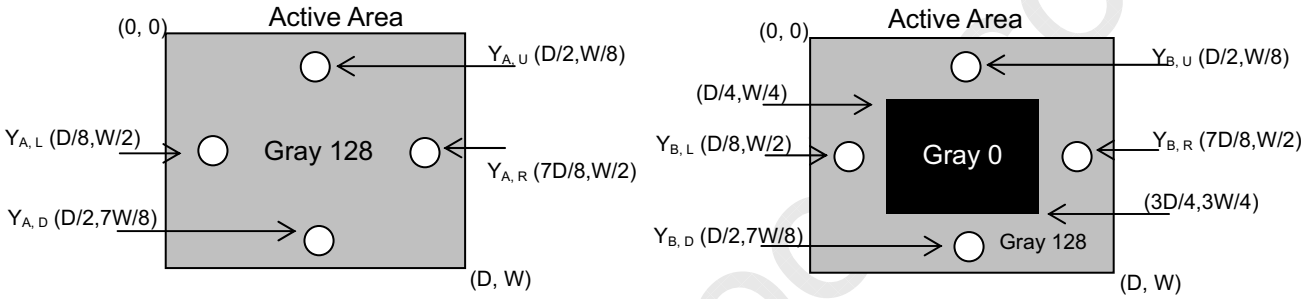
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

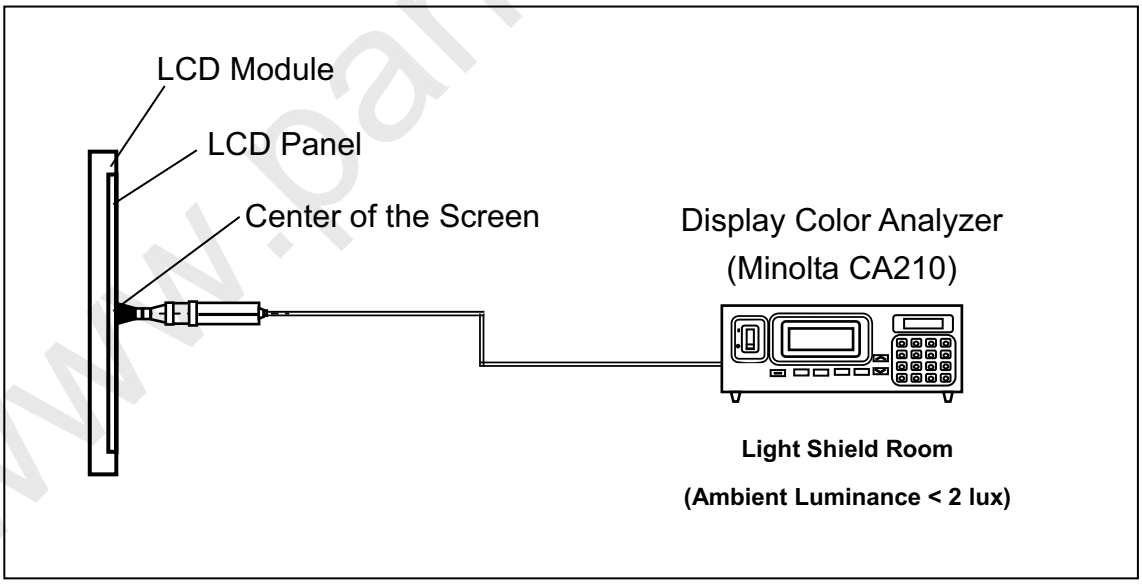
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

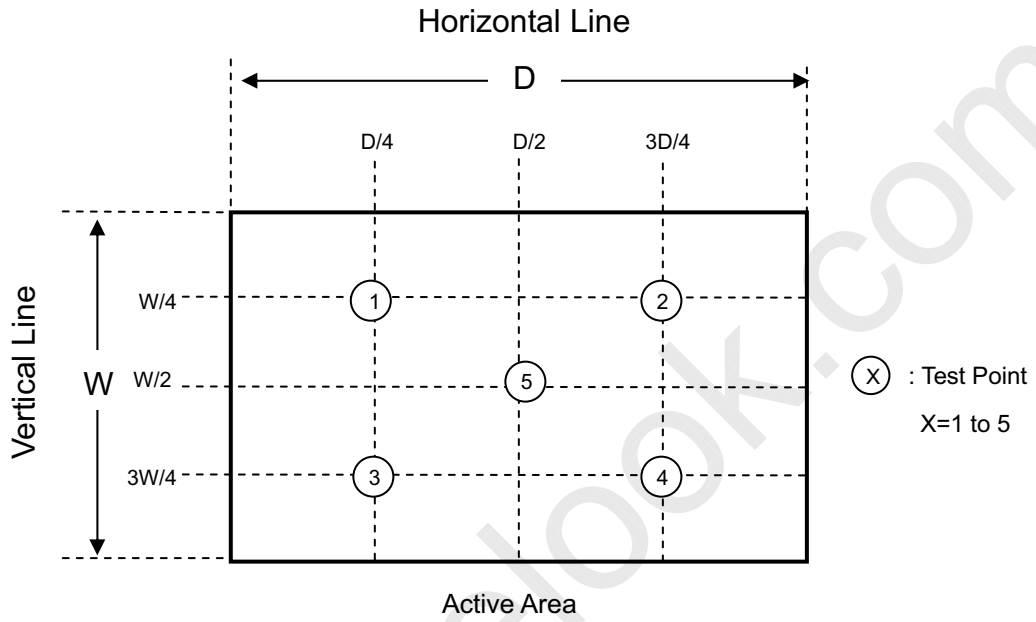
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

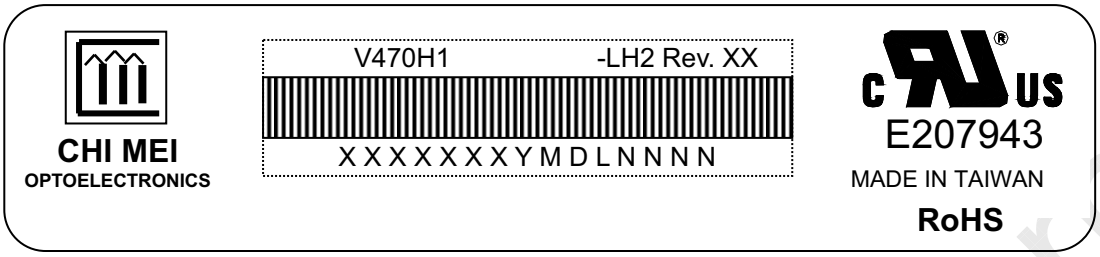
(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

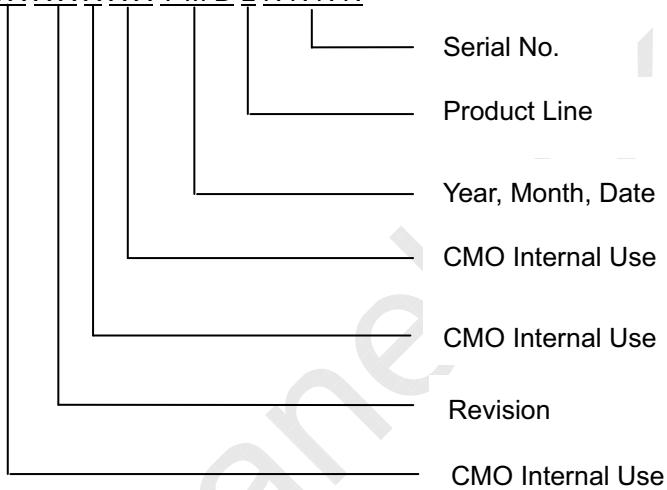
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V470H1-LH2

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1190(L)x280(W)x712(H)mm

(3) Weight : approximately 52Kg (3 modules per box)

(4) Desiccant (Drier) : Weight 30g / 1 piece, Quantity 3 pcs, Cobalt chloride free

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

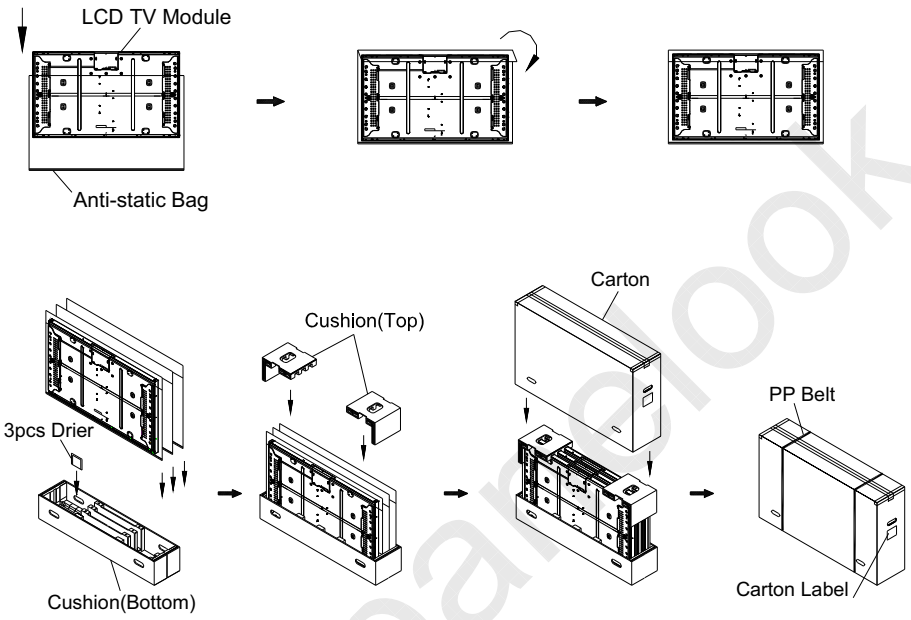
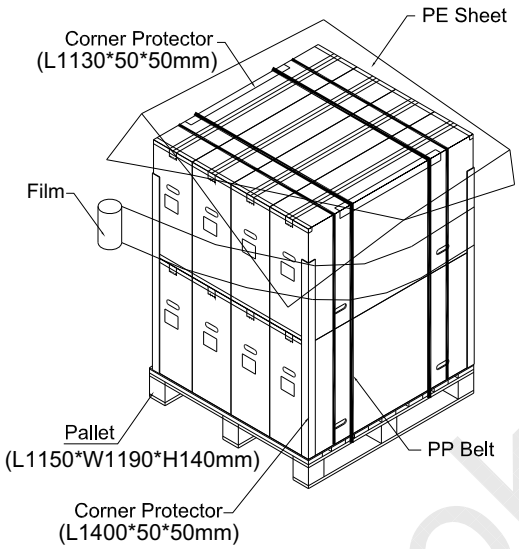


Figure.10-1 | Figure.9-1 packing method

Air Transportation &

Sea / Land Transportation (40ft Container)



Sea / Land Transportation (40ft HQ Container)

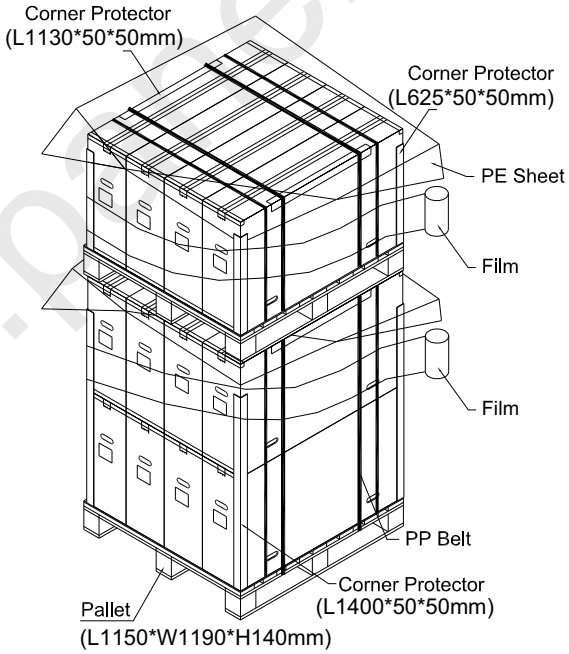


Figure.10-2 packing

11. MECHANICAL CHARACTERISTIC